61 THE CHIPS TO SYSTEMS CONFERENCE

SHAPING THE NEXT GENERATION OF ELECTRONICS

JUNE 23-27, 2024

MOSCONE WEST CENTER
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Automated – BUS Routing Solution for Efficient DRC Clean TestChip Design

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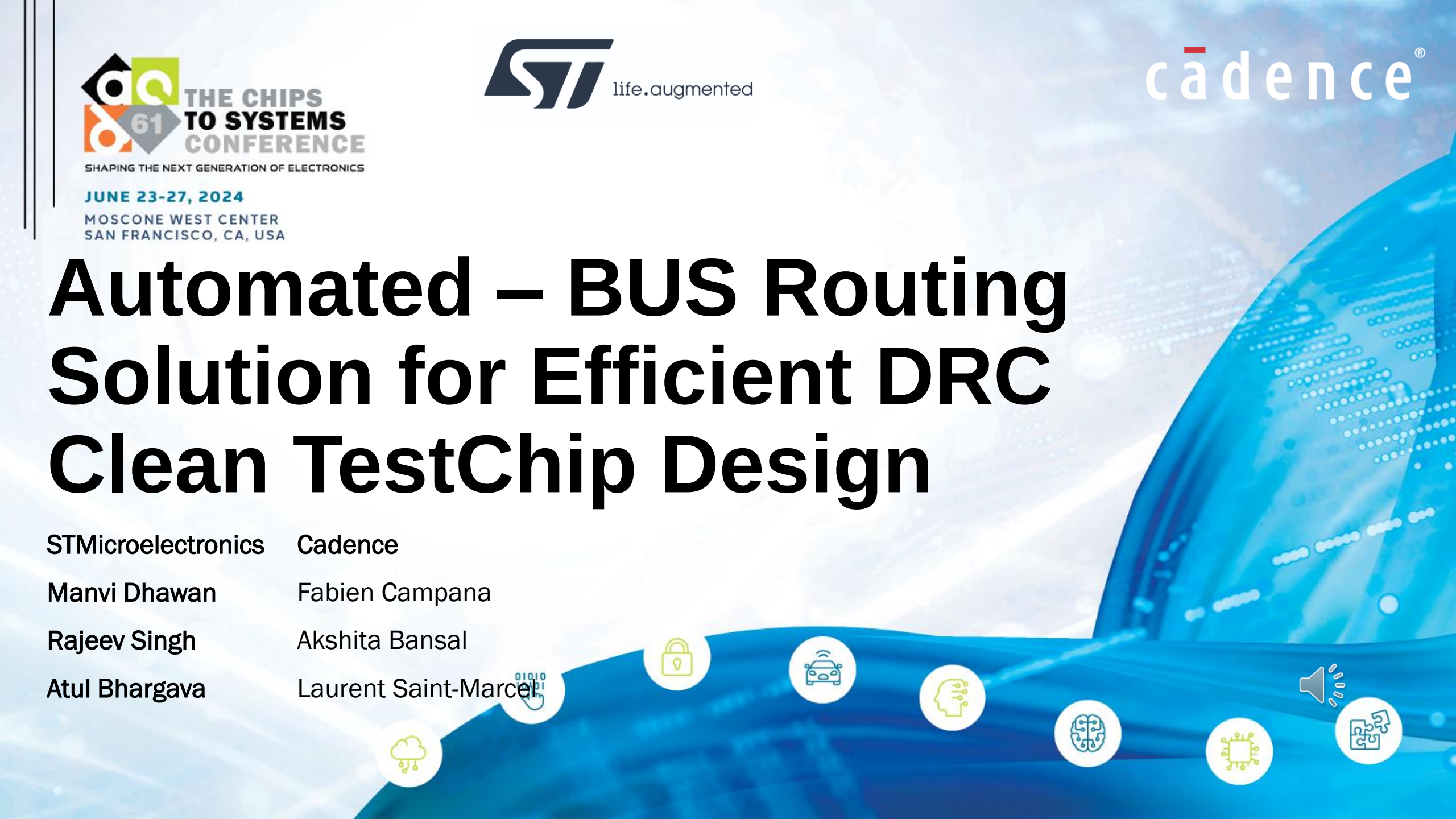
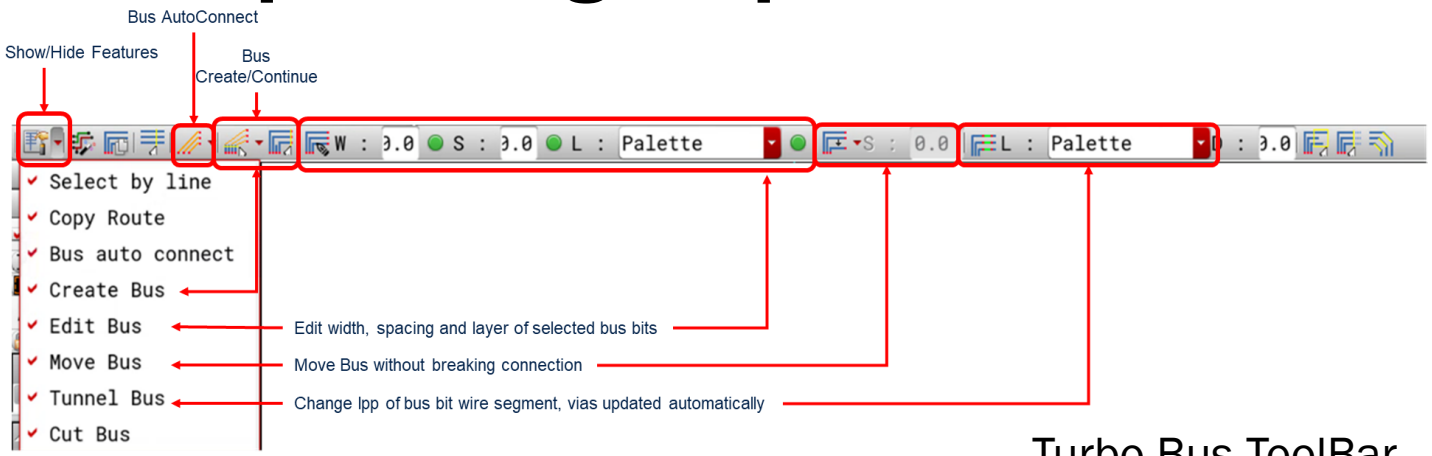
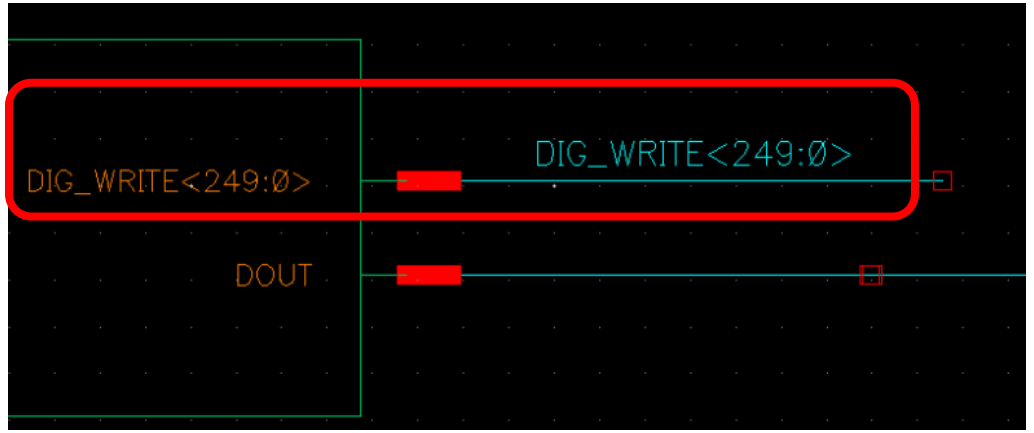


TestChip Routing Requirements

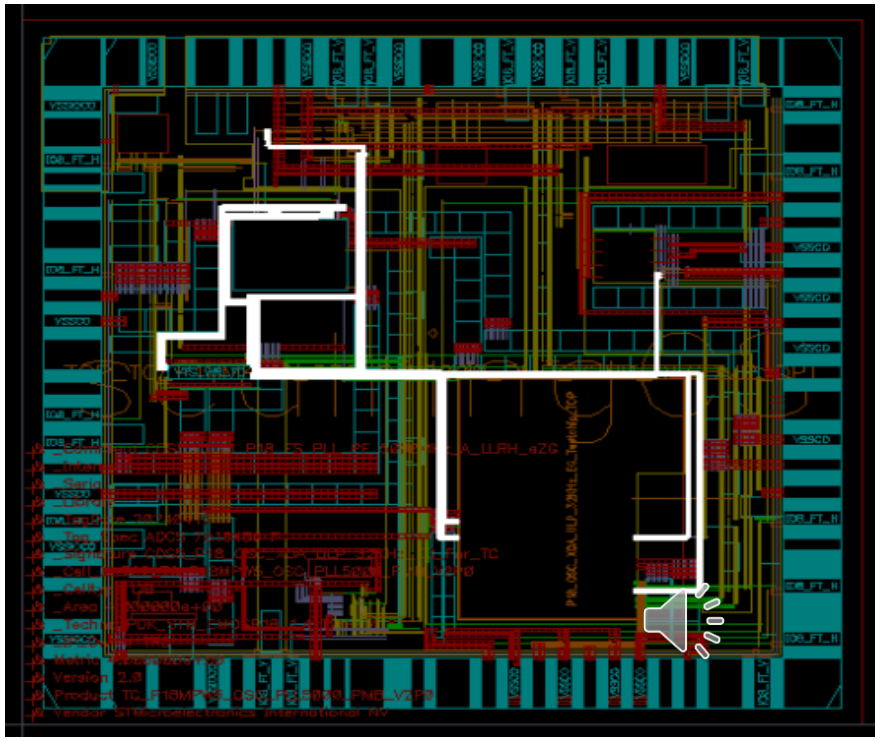


Turbo Bus ToolBar



Testchip block with large bus (250 bits)

- **Critical nets** (CLK/POWER) need to be **completed before routing other nets**
  - Full control of bus topology
- Efficient Automatic **bus connect for order of 200s bits**
- Bus continue from **hierarchical pins** in case block-to-block, block-to-pins connections
- Editing of bus once the routing is already done for **ECO updates and DRC fixes**
  - **Vias should be updated automatically** to maximize cuts for overlap



Sample block connections for a block at top level in Testchip

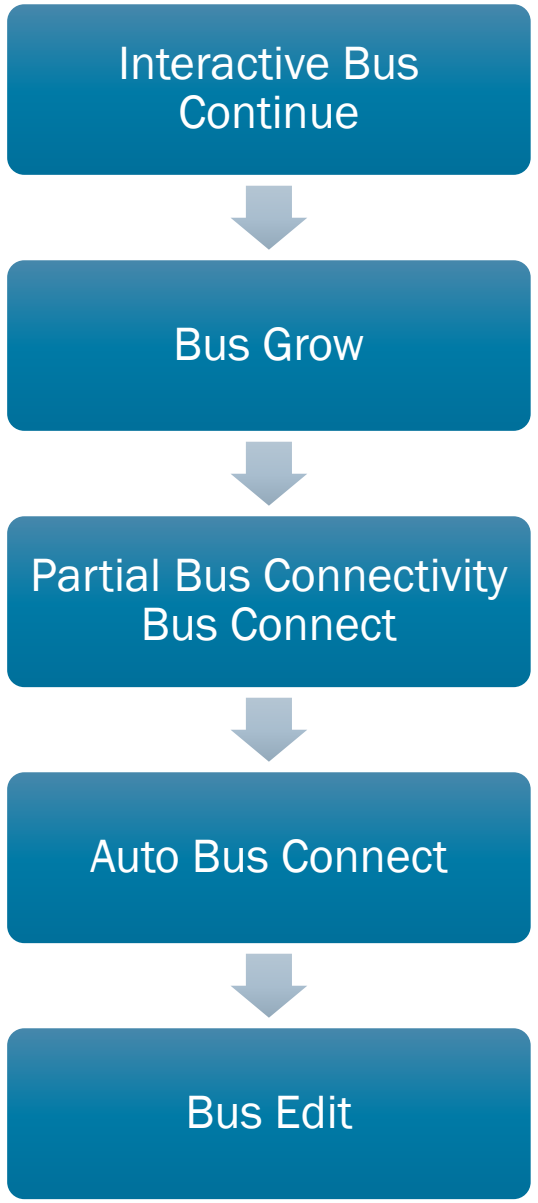
Automatic Routing Flow

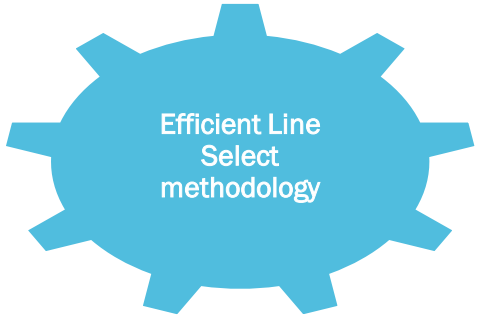
- New Fast & intuitive create/edit bus command use model

- New Topology *Copy* command
  ➔ smarter than regular copy commands

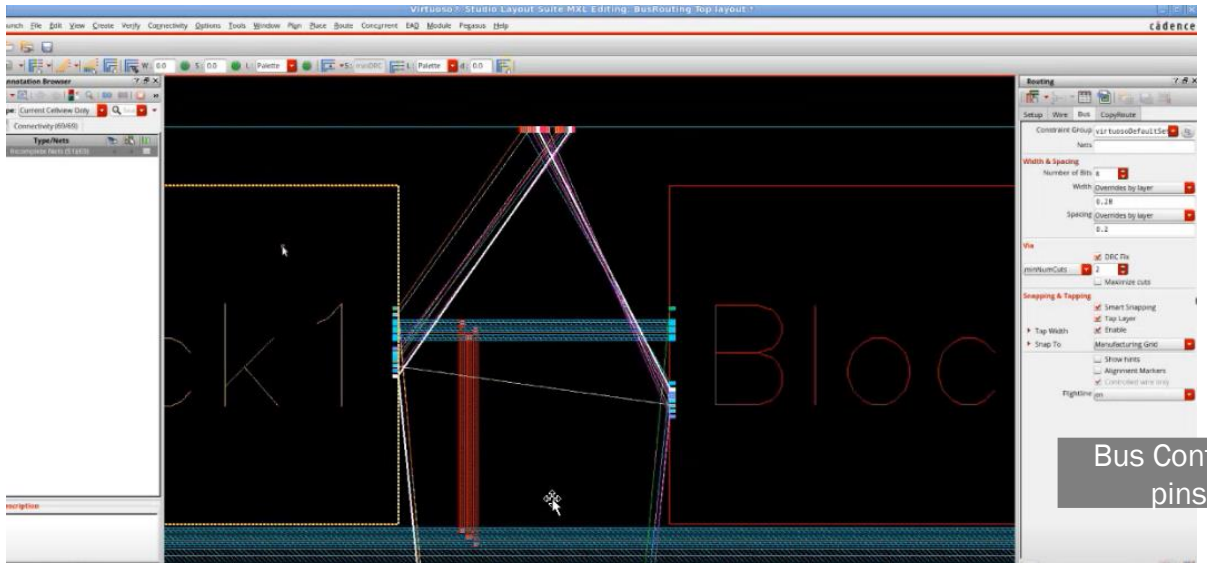
- Tool support automatic connections without connectivity (required for predefinition of paths for assisted routes)
  ➔ support more cases than regular routers

- New "all in one go" use model:
  ➔ tools automatically adjust routing parameters based on target objects to speed-up the edition
  ➔ no manual post adjustments

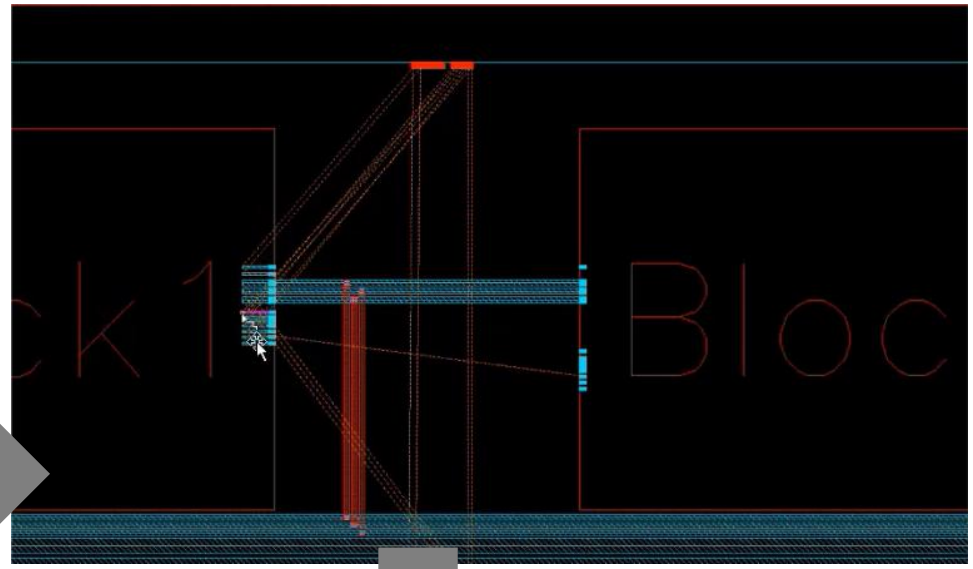


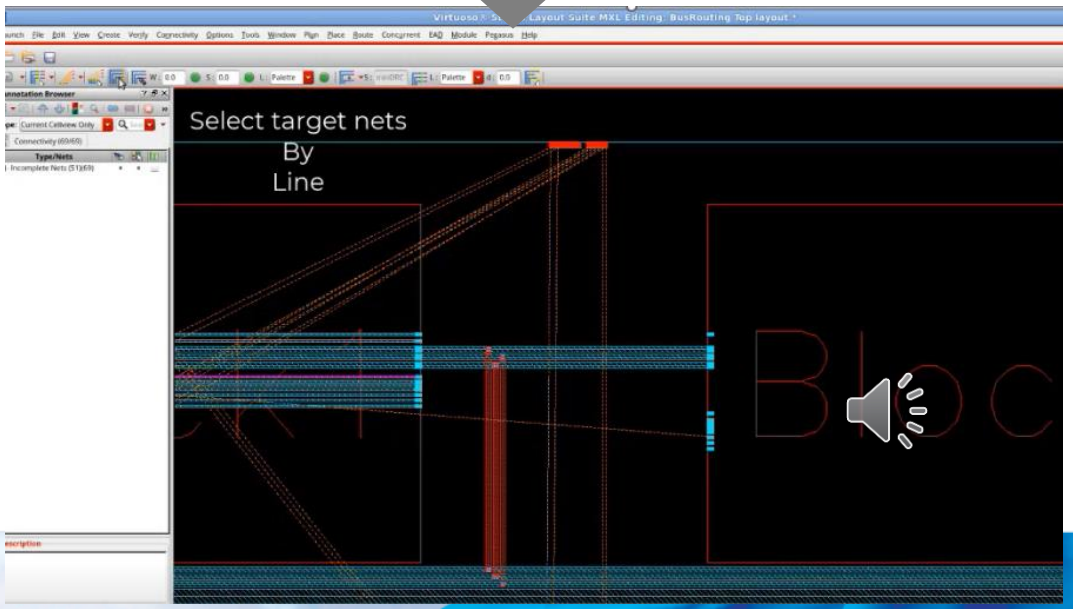


Block to Block Connection

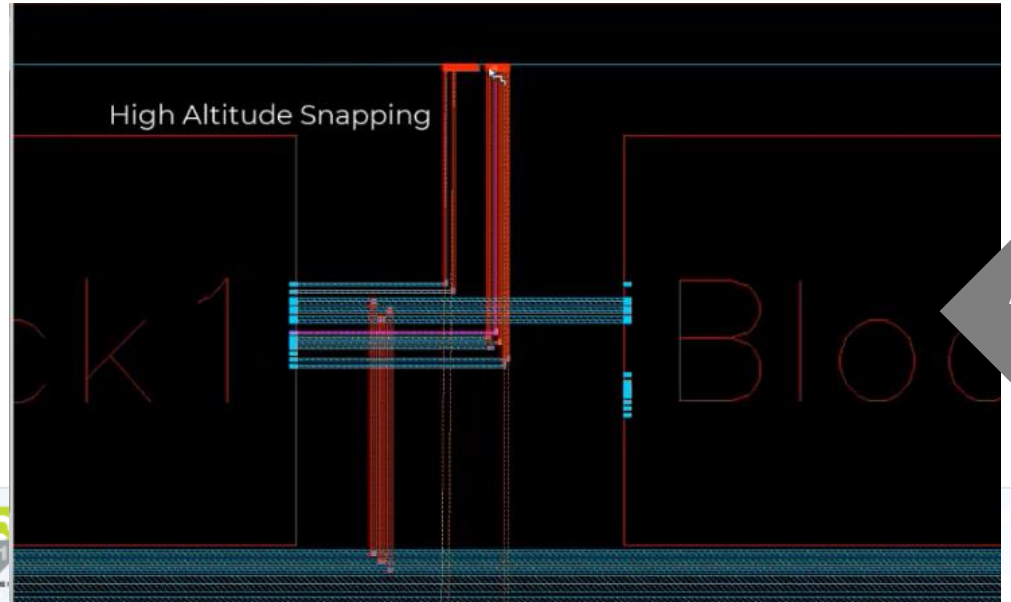


Bus Continue from pins in L-1



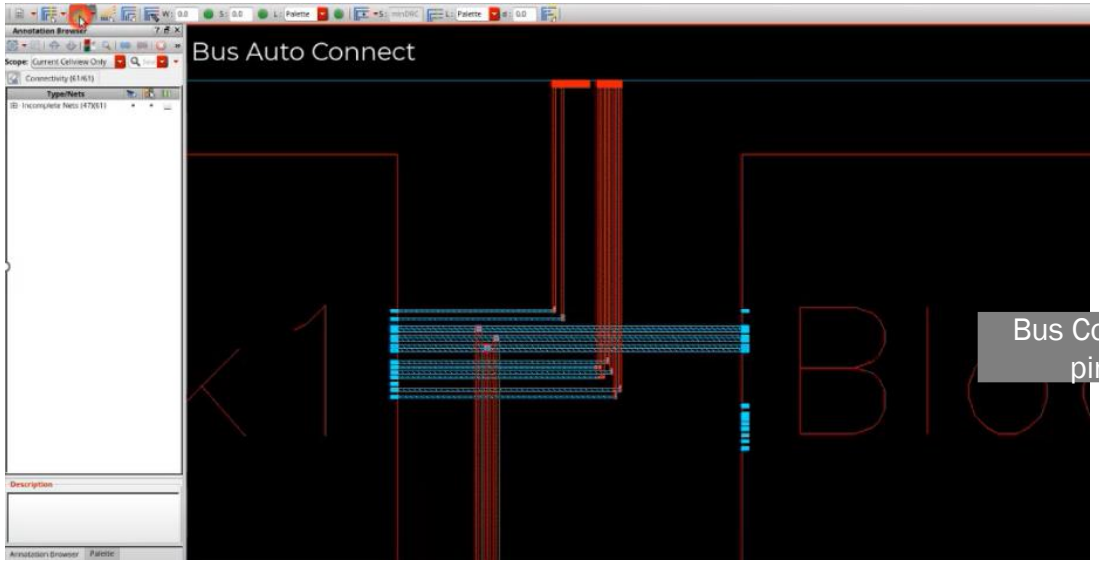


Auto Snapping to target bits



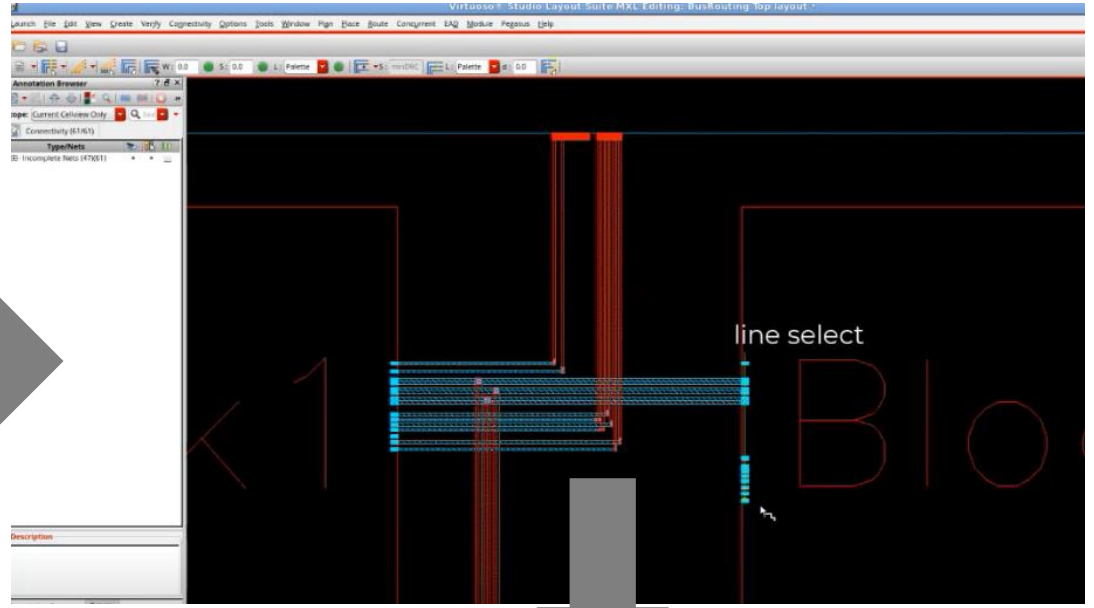
Bus autoconnect

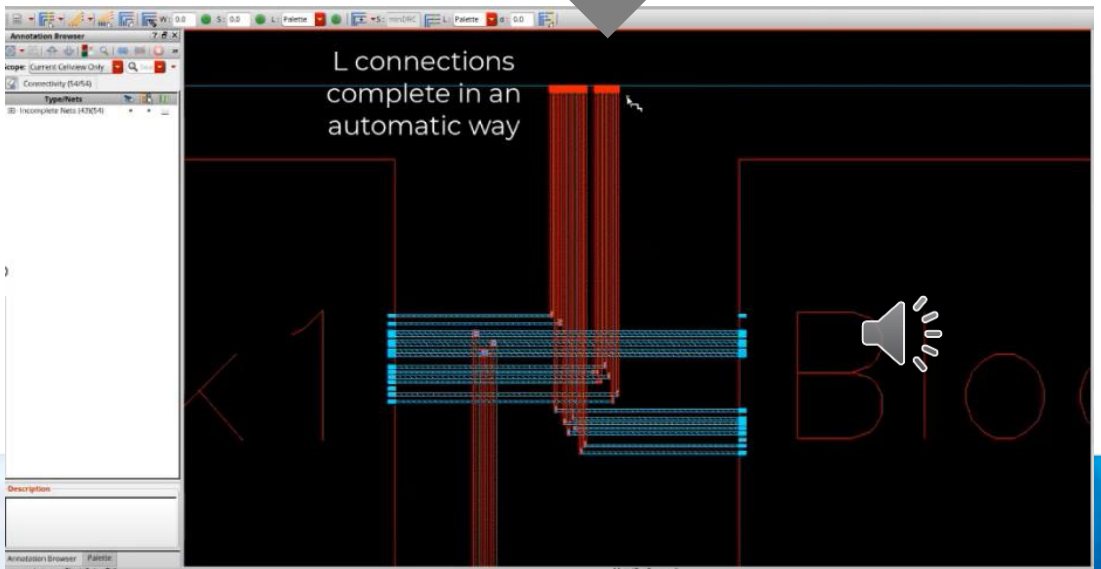
No need to drag wires, auto-connect of source and target by click of button



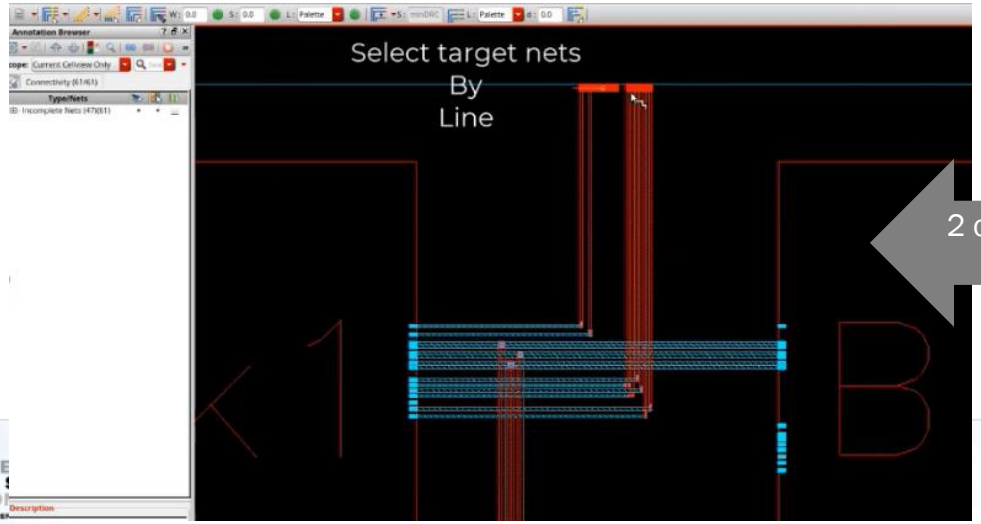
Bus Continue from pins in L-1

Source Selection



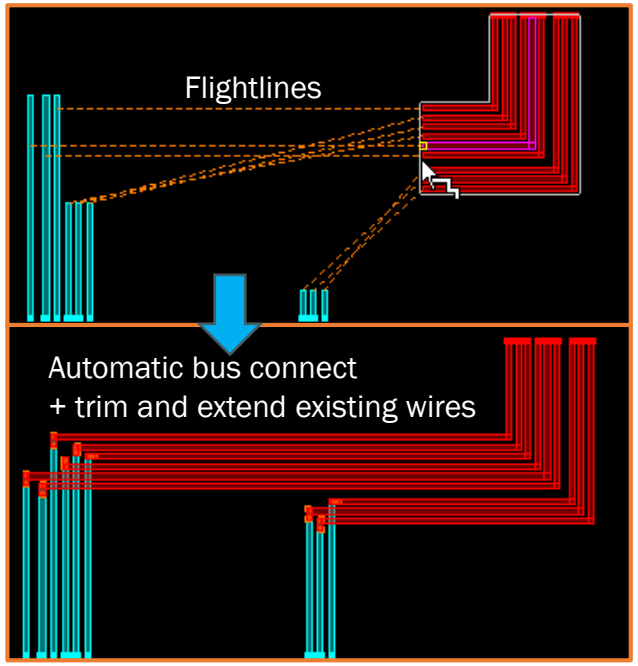


2 click bus auto connect



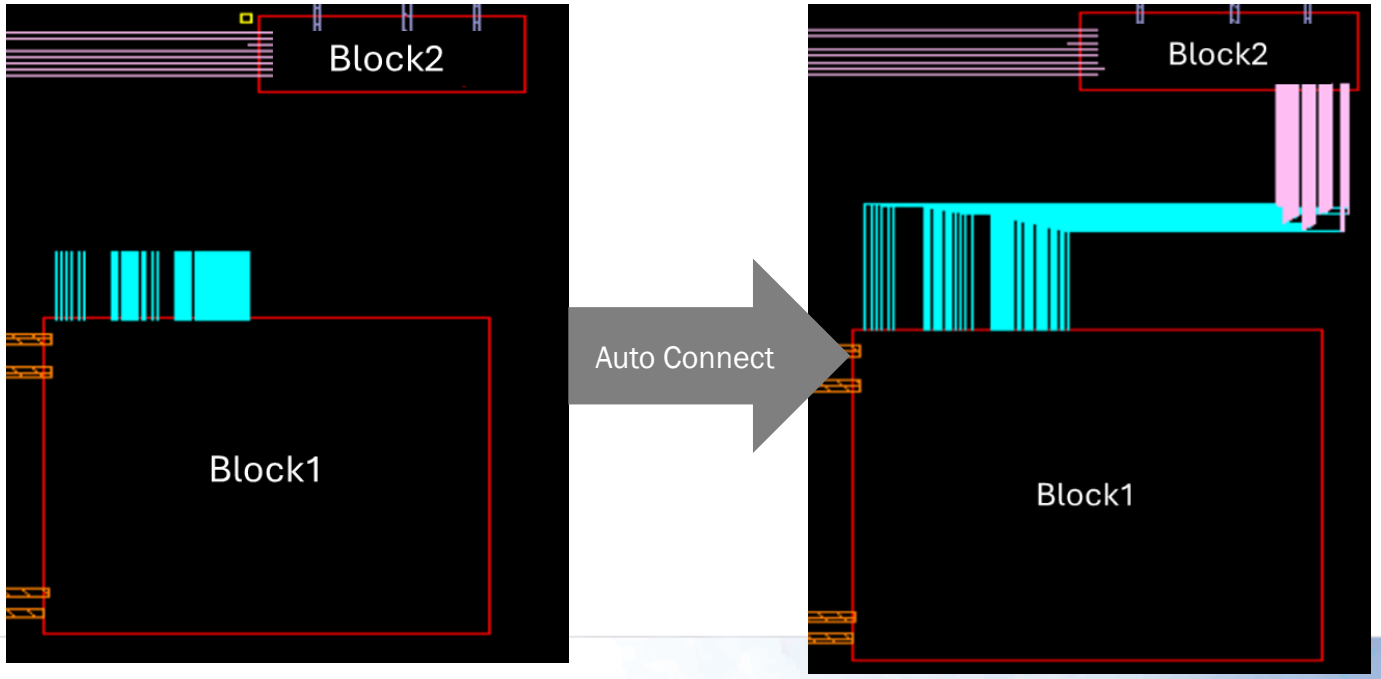
Bus Continue from hierarchy

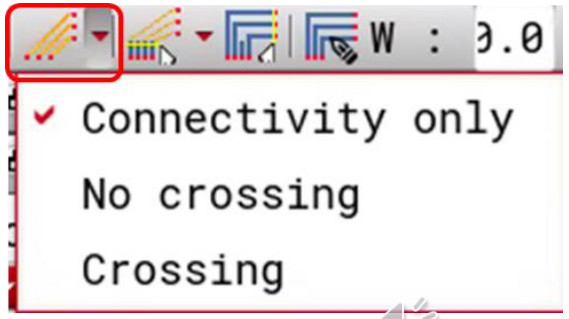
- Dynamic update of spacing between intermediate bits
- Auto trim and extend as per target bit snapping
- No need to zoom in and align individual bits



Auto Bus Connect based on Connectivity

Works with and without connectivity

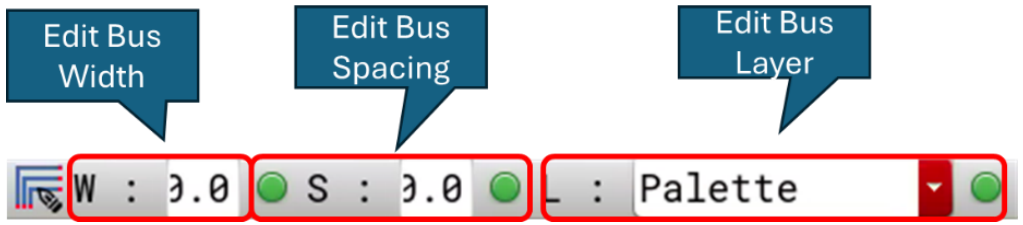


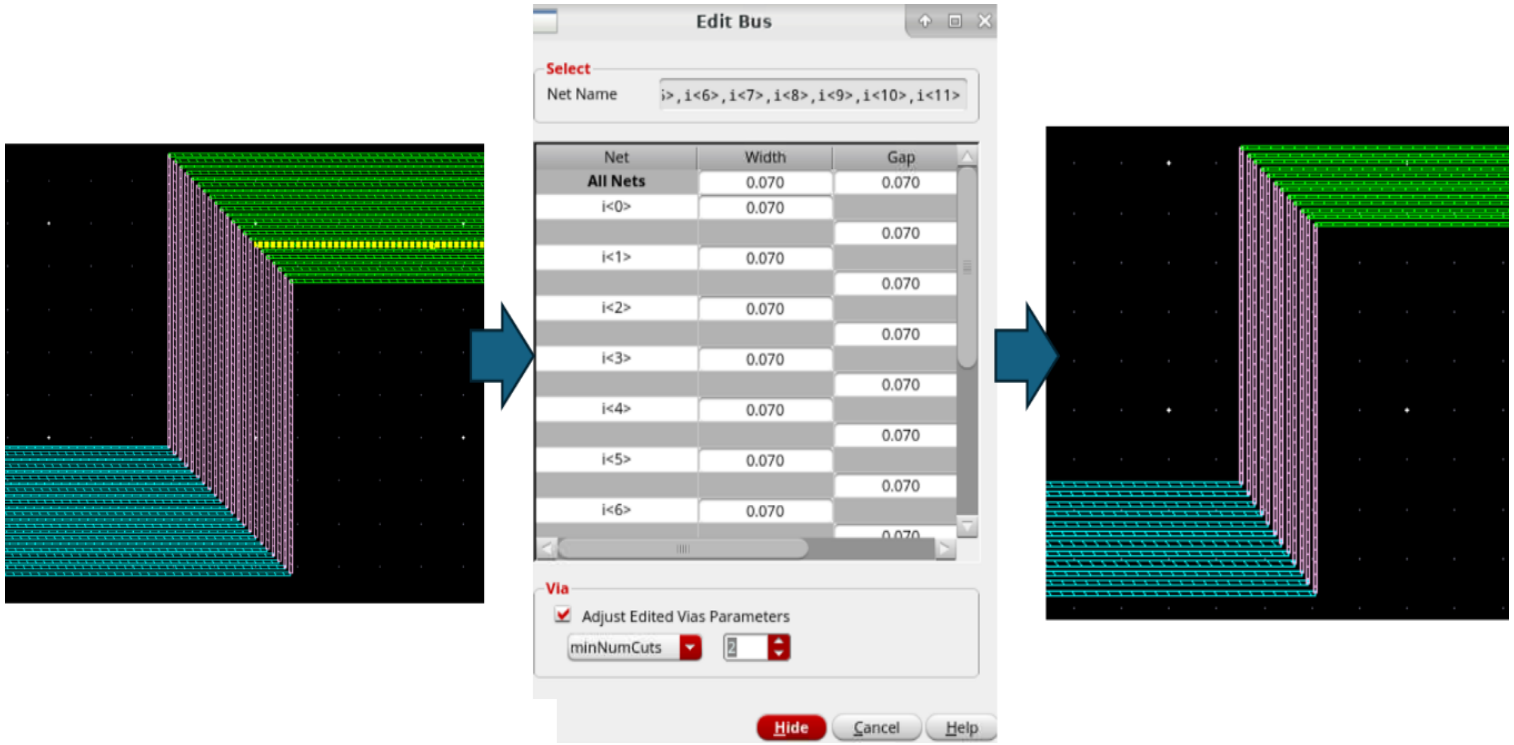


Auto Bus Connect Options

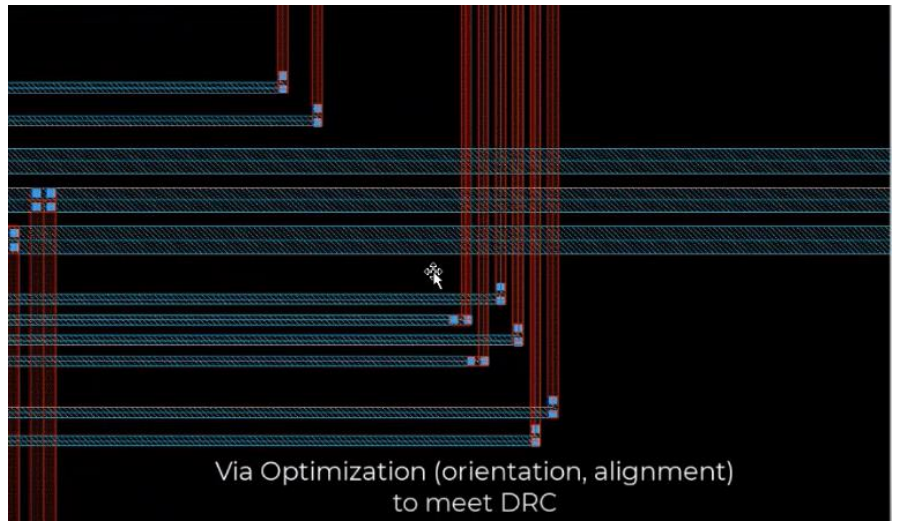
Bus Edit

- Bus updates are easy with Edit but commands





Update Bus after Generation

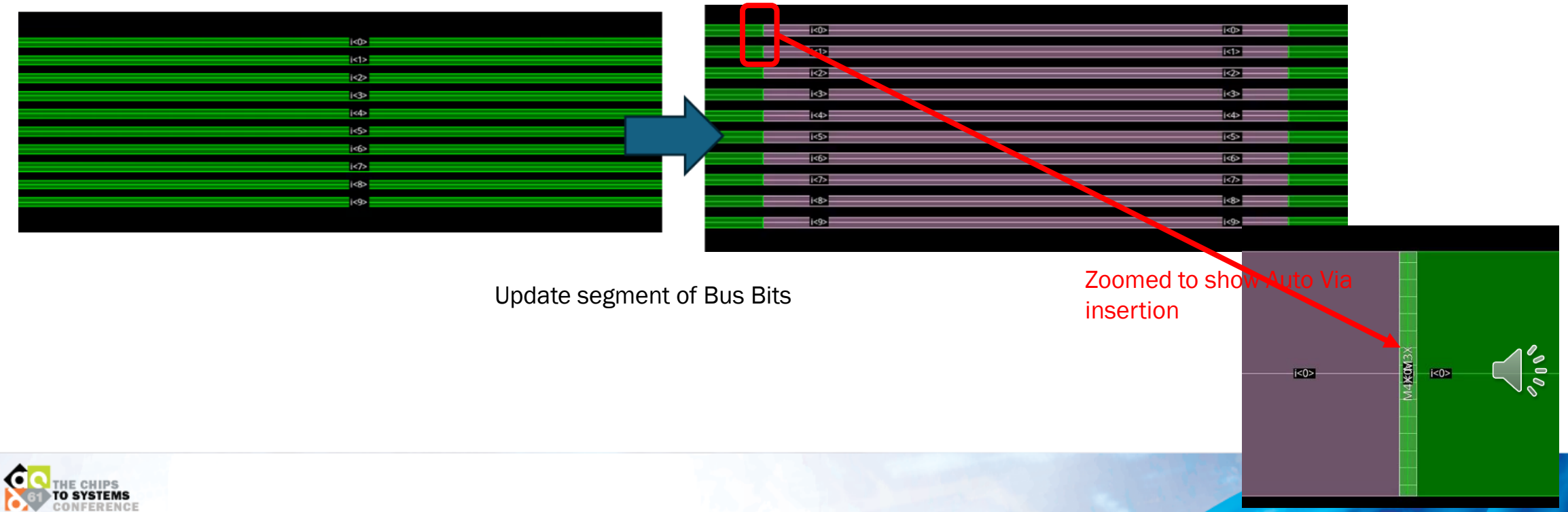


Vias are optimized automatically to ensure DRC correct result

Bus Tunneling

- Bus Layer can be changed for entire bit or partial segment
- Vias are automatically created based on min number of cuts specified in Interactive Routing Assistant
- Via alignment and number of cuts are managed by tool automatically

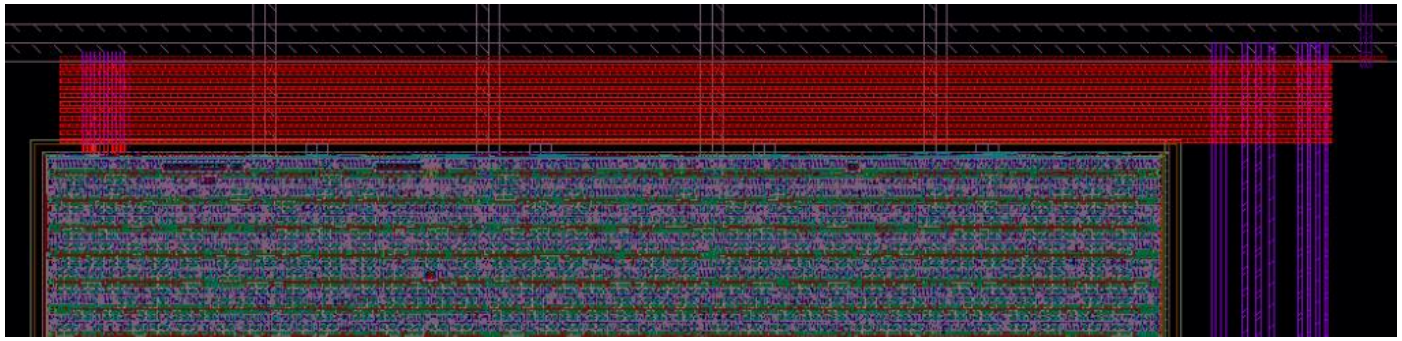
Turbo Bus Tunnel



Update segment of Bus Bits

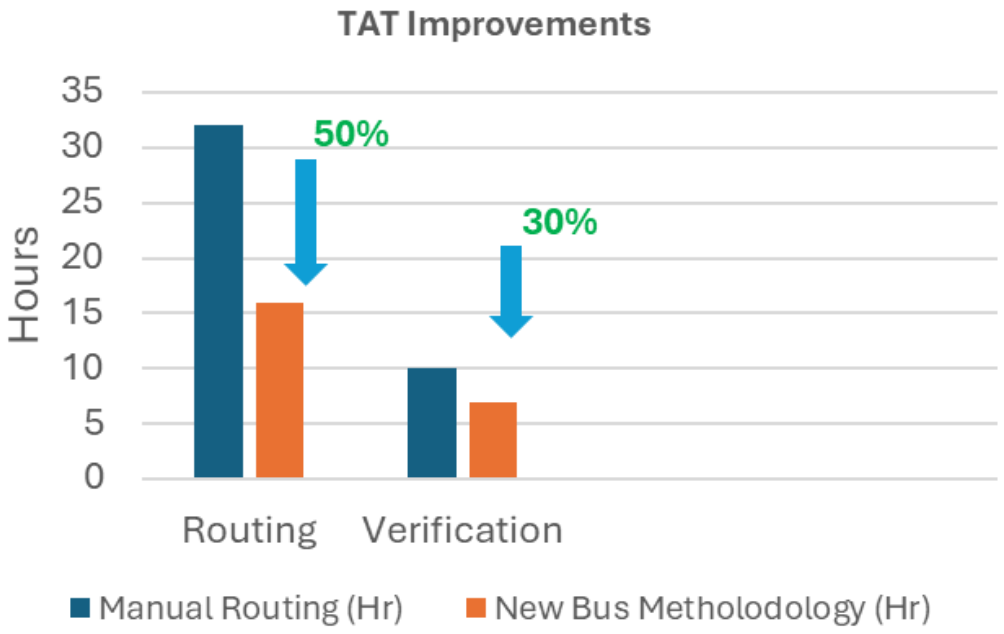
Results & Summary

- Implemented with 18nm, 130nm technologies, with approx. ~300 connections
  - Solution is **Technology Independent**



Bus Routing Structure in TestChip

- 50% Gain in term of routing vs manual solution
- 30% Gain for the verification as DRC clean by construction



Auto Bus Connect with block-to-block connections